IN THE SPECIFICATION:

Please amend the specification as follows:

Please amend the paragraph on page 6, from lines 1 through 2, as follows:

FIG. 12 is a block diagram showing an example of a [[an]] configuration provided with two-stage registers; [[:]]

Please amend the paragraph on page 10, from lines 8 through 19, as follows:

A row address predecoder RPD [[XPD]] predecodes the row address and outputs a row predecoder address RPA to the row decoder RDEC. The row decoder RDEC further decodes the row predecoder address. According to the decoding, the word driver WD selectively drives a word line in the memory cell array MCA. A column address predecoder CPD [[YPD]] predecodes the column address and outputs a column predecode address CPA to the column decoder CDEC. The column decoder CDEC further decodes the column predecode address CPA. According to the decoding, the column selector CSEL selectively connects a bit line in the memory cell array MCA to an input output line IO.

Please amend the paragraph bridging pages 13 and 14, from line 6 on page 13 through line 4 on page 14, as follows:

FIG. 4 is an example of a configuration of the write buffer block WB in FIG. 1. It comprises a write pulse generator WPG and two write buffers WB1s. Also in this example, write is concurrently performed to two memory cells in the memory cell array. The number of memory cells to which write is concurrently done can be changed by changing the number of write buffers WB1s accordingly. The write pulse generator WPG generates resistivity-lowering and resistivity-raising pulses and outputs them respectively to write pulse lines WP0 and WP1. Each write buffer WB1 has three inverters, two two-input NAND gates and two CMOS path gates each composed of two NMOS transistors MNC1, MNC0 and two PMOS transistors MPC1, MPC0. If enabled by a write instruction signal WRIT, the write buffer block WB respectively connects the input output lines IO0 and IO1 to the write pulse line WP0 or WP1 according to the write data DI0 and DI1. The CMOS path gates used therein allows the input and output lines IO0 and IO1 to be driven to the ground voltage at their falling edges by the write pulse generator WPG. This can sharpen the falling edge of the pulse waveform of the bit line current to realize stable write operation since the charge

accumulated to the parasitic capacitance of the input and output line is prevented from discharging through the bit line and memory cell.

Please amend the paragraph bridging pages 15 and 16, from line 10 on page 15 through line 1 on page 16, as follows:

FIG. 6 shows another example of a configuration of the flag register FR. It comprises a set-reset latch SRL, an inverter, a shot pulse generator SPG composed of two inverters and a two-input NAND gates [[gate]], and a delay circuit DLY. The write instruction signal WRIT sets the latch SRL which in turn sets the flag FLG to '1'. Thereafter, the feedback signal WFB output from the delay circuit DLY resets the latch SRL which in turn resets the flag FLG to '0'. The delay circuit DLY is designed to provide a delay time during which stable read operation becomes possible from a memory cell after a resistivity-raising pulse is applied to the phase change resistor therein. In addition, the delay time is scaled so as to make the pulse width of the feedback signal WFB narrower than that of the write instruction signal WRIT. This prevents the write instruction signal WRIT and feedback signal WFB from becoming '1' simultaneously, which may cause the flag register FLG to malfunction.

Please amend the paragraphs on pages 18 and 19, from line 4 on page 18 through line 12 on page 19, as follows:

FIG. 8 shows an example of the timing sequence for a read operation. As with the write operation shown in FIG. 7, the word line WL is switched in response to a transition of the external address ADR. If the flag FLG is '1', a pulse on the address transition signal AT activates the address comparator ACP to compare the internal address AI with the retained write address AS and output the result on the address hit signal AH. If the address hit signal AH is '0', a read voltage VRED is supplied to the selected bit line BL for a desirable period by the sense amplifier via the input output line IO and column selector CSEL while data distinction is performed based on the magnitude of the flowing current. The read data DO, output from the sense amplifier block, is output by the data selector DOS as output data DS. If the address hit signal AH is '1', the sense amplifier remains in the standby state to keep the bit line BL to the ground voltage VSS. The data selector DOS outputs the retained write data DR as output data DS. When the chip select bar signal CSb and output enable bar signal OEb [[WEb]], parts of the command signal CMD, fall to the low level, the output buffer is activated to drive the input output data DQ to the output level Dout according to the output data DS. When either the chip select bar signal CSb or the output ~~write~~ enable bar signal

OEb [[WEb]] rises to the high level to terminate the read operation period, the output buffer DOB is forced into the high impedance state.

By controlling the voltage supply to the bit line by the address hit signal AH as mentioned above, it is possible to prevent the phase change resistor ~~resister~~ from becoming unstable by a voltage which otherwise may be applied thereto immediately after the resistivity is raised. This is effective also when the memory is used as an asynchronous SRAM since address comparison can be controlled on an each address transition basis by using the address transition detector.

Please amend the paragraph bridging pages 19 and 20, from line 14 on page 19 through line 8 on page 20, as follows:

FIG. 9 is a block diagram of a key portion of a synchronous phase change memory configured in accordance with the present invention. Generally, a synchronous phase change memory takes in a command and address and performs an operation based on an external clock signal. As with the embodiment of an asynchronous phase change memory, shown in FIG. 1, this synchronous phase change memory of the present invention, shown in FIG. 9 ~~there~~, includes a write data register DIR, an output data selector DOS, a write address register AR, an address comparator ACP and a flag register FR. It also includes a clock buffer CKB, a command buffer CB, a command decoder CD, an address buffer AB, a row predecoder RPD, a column predecoder CPD, an input buffer DIB, an output buffer DOB, a sense amplifier block SA and a write buffer block WB. Further, a memory cell array MCA is formed with a row decoder RDEC, a word driver WD, a column decoder CDEC and a column selector CSEL. The memory cell array MCA has the same configuration as shown in FIG. 2. Although only one memory cell array MCA is shown in FIG. 9, a plurality of memory cell arrays MCAs may be included.

Please amend the paragraph on page 21, from lines 3 through 14, as follows:

A row address predecoder RPD [[XPD]] predecodes the row address and outputs a row predecoder address RPA to the row decoder RDEC. The row decoder RDEC further decodes the row predecoder address. According to the decoding, the word driver WD selectively drives a word line in the memory cell array MCA. A column address predecoder CPD [[YPD]] predecodes the column address and outputs a column predecode address CPA to the column decoder CDEC. The column decoder CDEC further decodes the column predecode address CPA. According to the decoding, the column selector CSEL selectively

connects a bit line in the memory cell array MCA to an input output line IO.

Please amend the paragraph bridging pages 22 and 23, from line 20 on page 22 through line 4 on page 23, as follows:

Unlike the asynchronous operation shown in FIG. 7, the valid input Din is taken in simultaneously with the write command. Therefore, when the input Din is '0', it is possible to drive the bit line BL to the set voltage VSET long enough [[long]] to lower the resistivity of the phase change resistor. When the input Din is '1', since the bit line BL can immediately be driven to the reset voltage VRST, the resistivity of the phase change resistor can be raised earlier. Therefore, after the resistivity is raised, a longer time interval can be secured before the subsequent read operation from that memory cell.

Please amend the paragraph bridging pages 24 and 25, from line 14 on page 24 through line 18 page 25, as follows:

FIG. 12 is a block diagram of another example of an asynchronous phase change memory configured in accordance with the present invention. It is characterized in that a first write data register DIR1 and a second write data register DIR2 are provided to form a two-stage write data register and likewise a first write address register AR1 and a second write address register AR2 form a two-stage ~~two-state~~ write address register. An address comparator AC2 compares the internal address AI with the first retained write address AS1 and second retained write address AS2 and outputs an address hit signal AH2 indicating whether the internal address AI agrees with them. Controlled by the address hit signal AH2, an output data selector DS3 selects output data DS from the readout data DO, first retained write data DR1 and second retained write data DR2 and outputs the output data DS. If the internal address AI agrees with the first retained write address AS1, the first retained write data DR1 is selected. If the internal address AI agrees with not the first retained write address AS1 but the second retained write address AS2, the second retained write data DR2 [[DR1]] is selected. If the internal address AI agrees with neither the first retained write address AS1 nor the second retained write address AS2, the readout data DO is selected. Note that if write operations are successively performed to the same address, the first retained write address AS1 becomes equal to the second retained write address AS2 and therefore the internal address AI agrees with both. In this case, the output data selector DS3 selects the first retained write data DR1 which was entered later.

Please amend the paragraph on page 26, from lines 17 through 23, as follows:

Although this embodiment is an asynchronous phase change memory, such a synchronous phase change memory as shown in FIG. 9 can also be configured to have a two-stage write data register and a two-stage write address register. This configuration can also make ~~makes~~ longer the period between a write operation to a memory cell and the subsequent read operation from the same memory cell.

Please amend the paragraph on pages 26 through 28, from line 25 on page 26 through line 10 on page 28, as follows:

FIG. 13 is a block diagram of a key portion of another asynchronous phase change memory configured in accordance with the present invention. This embodiment is characterized by its write operation called a late write. Similar to the embodiment shown in FIG. 12, a first write data register DRL and a second write data register DRD are provided to form a two-stage write data register and likewise a first write address register ARL and a second write address register ARD form a two-stage ~~two-state~~ write address register. Unlike the embodiment of FIG. 12, however, the first write data register DRL and first write address register ARL are provided for late write operation. An address selector ASL is provided to output the internal address AI or the first retained write address AL to a row predecoder RPD and column predecoder CPD as a selected address A0. The internal address AI is selected for a read operation whereas the first retained write address AL is for a write operation. The first retained write data DL is also sent to a write buffer block WB. As with the embodiment of FIG. 12, an address comparator AC2 compares the internal address AI with the first retained write address AL and the second retained write address AD and outputs an address hit signal AH2 indicating whether the internal address AI agrees with them. Controlled by the address hit signal AH2, an output data selector DS3 selects output data DS from the readout data DO, first retained write data DL and second retained write data DD and outputs the output data DS. This asynchronous phase change memory also includes a flag register FR, a command buffer CB, a control signal generator CPGL, an address buffer AB, an address transition detector ATD, a row predecoder RPD, a column predecoder CPD, an input buffer DIB, an output buffer DOB, a sense amplifier block SA and a write buffer block WB. Further, it has a memory cell array MCA provided with a row decoder RDEC, a word driver WD, a column decoder CDEC and a column selector CSEL. They operate as described with FIG. 1.

Please amend the paragraph bridging pages 30 and 31, from line 23 on page 30 through line 6 on page 31, as follows:

The following describes an example of an application of a phase change memory in accordance with the present invention. FIG. 15 is an example of a configuration of a flash memory card. A flash memory card FMC has a plurality of large capacity flash memories LFMs [[LMFs]], a memory controller MCT and a phase change memory PMC. By using the phase change memory PMC as a buffer, the memory controller MCT exchanges signals with the external and controls the large capacity flash memories LFMs [[LMFs]].